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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

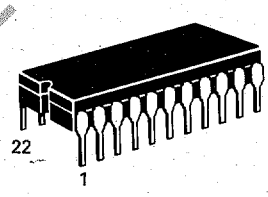
Military 93422
93L422,A

TTL 256 x 4-Bit Random Access Memory

The 93422 Series are 1024-bit Read/Write RAMs, organized 256 words by 4 bits, designed for high performance main memory and control storage applications.

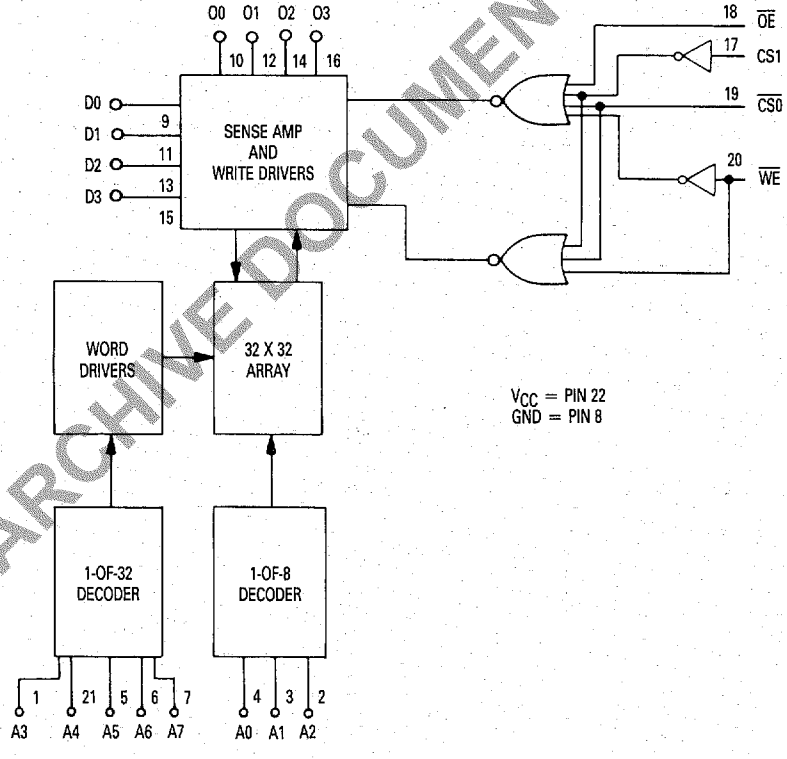
They have full decoding on-chip, separate data input and data output lines, an active low-output enable, write enable, and two chip selects, one active high, one active low. These memories are fully compatible with standard TTL logic families. A three-state output is provided to drive bus-organized systems and/or highly capacitive loads.

- Three-State Outputs
- Non-Inverting Data Outputs
- Power Dissipation — 0.26 mW/Bit Typical
- Standard 22-Pin, 400 Mil Wide Package
- Power Dissipation Decreases with Increasing Temperature
- Organized 256 Words x 4 Bits
- Two Chip Select Lines for Memory Expansion
- Address Access Time: 93422 — 60 ns Max
  93L422A — 55 ns Max
  93L422 — 75 ns Max

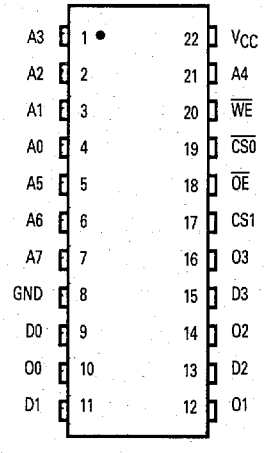


W SUFFIX
CASE 736-05
CERAMIC

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

$\overline{CS0}$, CS1	Chip Selects
A0–A7	Address Inputs
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
D0–D3	Data Inputs
O0–O3	Data Outputs

FUNCTIONAL DESCRIPTION

The 93422 Series are fully decoded 1024-bit random access memories organized 256 words by 4 bits. Word selections are achieved by means of an 8-bit address, A0–A7.

The Chip Select (CS0 and CS1) inputs provide for memory array expansion. For large memories, the fast chip select time permits the decoding of chip select from the address without increasing address access time.

The read and write operations are controlled by the state of the active low Write Enable (WE, Pin 20). With WE and CS0 held low and the CS1 held high, the data at D_n is written into the addressed location. To read, WE and CS1 are held high and CS0 is held low. Data in the specified location is presented at the output (O0–O2) and is non-inverted.

The three-state outputs provide drive capability for higher speeds with capacitive load systems. The third state (high impedance) allows bus-organized systems where multiple outputs are connected to a common bus.

During writing, the output is held in a high-impedance state.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature Ceramic Package (W Suffix)	−65°C to +150°C
Operating Junction Temperature, T_J Ceramic Package (W Suffix)	<165°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage (dc)	−0.5 V to +5.5 V
Voltage Applied to Outputs (Output High)	−0.5 V to +5.5 V
Output Current (dc) (Output Low)	+20 mA
Input Current (dc)	−12 mA to +5.0 mA

*Device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

GUARANTEED OPERATING RANGES

Part Number	Supply Voltage (V_{CC}) Min	Nom	Max	Ambient Temp. (T_A)
93422/BWAJC 93L422/BWAJC 93L422A/BWAJC	4.5 V	5.0 V	5.5 V	−55°C to +125°C

TRUTH TABLE

Inputs					Output	Mode
$\overline{OE}$	$\overline{CS0}$	CS1	$\overline{WE}$	D0–D3	O0–O3	
X	H	X	X	X	High Z	Not Selected
X	X	L	X	X	High Z	Not Selected
X	L	H	L	L	High Z	Write "0"
X	L	H	L	H	High Z	Write "1"
H	X	X	X	X	High Z	Output Disabled
L	L	H	H	X	O0–O3	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't Care (High or Low)

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range)

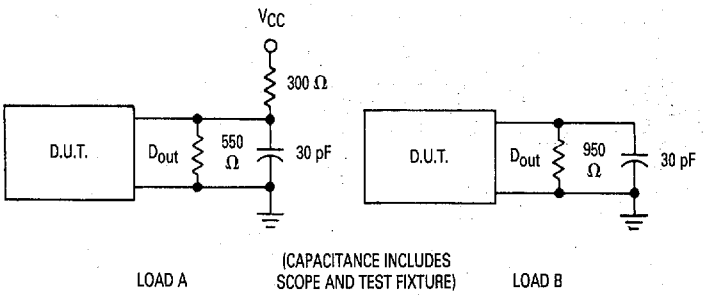
Symbol	Characteristic		Limits Min	Max	Units	Conditions	
V_{OL}	Output Low Voltage		—	0.45	Vdc	V_{CC} = Min, I_{OL} = 8.0 mA	
V_{IH}	Input High Voltage		2.1	—	Vdc	Guaranteed Input High Voltage for All Inputs	
V_{IL}	Input Low Voltage		—	0.8	Vdc	Guaranteed Input Low Voltage for All Inputs	
I_{IL}	Input Low Current		−0.01	−300	μAdc	V_{CC} = Max, V_{in} = 0.45 V	
I_{IH}	Input High Current		—	40	μAdc	V_{CC} = Max, V_{in} = 5.5 V	
I_{off}	Output Current (High Z)		— —	50 −50	μAdc	V_{CC} = Max, V_{out} = 2.4 V V_{CC} = Max, V_{out} = 0.45 V	
I_{OS}	Output Current Short Circuit to Ground		−10	−70	mAdc	V_{CC} = Max (Note 1)	
V_{OH}	Output High Voltage		2.4	—	Vdc	V_{CC} = Min, I_{OH} = −5.2 mA	
V_{IK}	Input Diode Clamp Voltage		—	−1.5	Vdc	V_{CC} = Max, I_{in} = −10 mA	
I_{CC}	Power Supply Current	93422	—	130	mAdc	T_A = +125°C	V_{CC} = 5.5 V, All Inputs Grounded
			—	155	mAdc	T_A = +25°C	
			—	170	mAdc	T_A = −55°C	
		93L422A 93L422	—	70	mAdc	T_A = +125°C	
			—	80	mAdc	T_A = +25°C	
			—	90	mAdc	T_A = −55°C	

AC OPERATING CONDITIONS AND CHARACTERISTICS

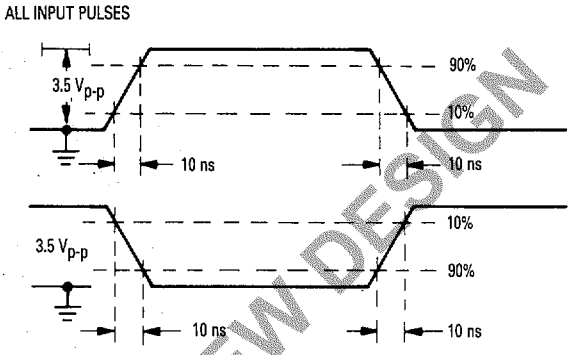
(Full operating voltage and temperature range)

AC TEST LOAD AND WAVEFORMS

LOADING CONDITIONS



INPUT PULSES



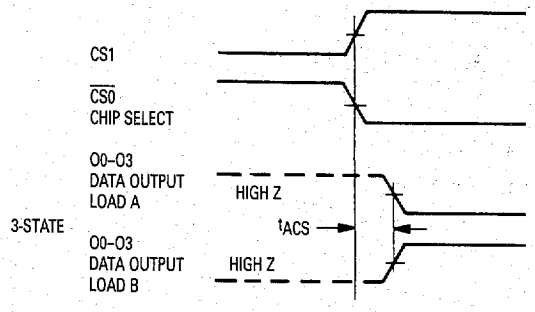
Symbol	Characteristic (Notes 1, 2, 3, 4, 5)	93422/BWAJC		93L422/BWAJC		93L422A/BWAJC		Unit
		Min	Max	Min	Max	Min	Max	
READ MODE	DELAY TIMES							ns
t_{ACS}	Chip Select Time	—	45	—	45	—	40	
t_{ZRCS}	Chip Select to High Z	—	45	—	45	—	40	
t_{AOS}	Output Enable Time	—	45	—	45	—	40	
t_{ZROS}	Output Enable to High Z	—	45	—	45	—	40	
t_{AA}	Address Access Time	—	60	—	75	—	55	
WRITE MODE	DELAY TIMES							ns
t_{ZWS}	Write Disable to High Z	—	45	—	45	—	45	
t_{WR}	Write Recovery Time	—	50	—	50	—	45	
	INPUT TIMING REQUIREMENTS							ns
t_W	Write Pulse Width (to guarantee write)	30	—	30	—	40	—	
t_{WSD}	Data Setup Time Prior to Write	5.0	—	5.0	—	5.0	—	
t_{WHD}	Data Hold Time After Write	5.0	—	5.0	—	5.0	—	
t_{WSA}	Address Setup Time (at t_W = Min)	10	—	10	—	10	—	
t_{WHA}	Address Hold Time	10	—	10	—	5.0	—	
t_{WSCS}	Chip Select Setup Time	5.0	—	5.0	—	5.0	—	
t_{WHCS}	Chip Select Hold Time	5.0	—	5.0	—	5.0	—	

NOTES:
1. Output short circuit conditions must not exceed 1.0 second duration.
2. The maximum address access time is guaranteed to be the worst-case bit in the memory.
3. Load A used to measure transitions between logic levels and from High Z state to logic Low state.
   Load B used to measure transitions between High Z state to logic High state.
   Load C used to measure transitions from either logic High or Low state to High Z state.
4. All time measurements are referenced to +1.5 Vdc except transitions into the High Z state where outputs are referenced to a delta of 0.5 Vdc from the logic level using Load C.
5. See test circuit and waveforms.

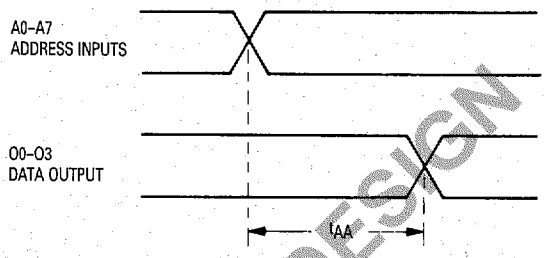
READ OPERATION TIMING DIAGRAM

(All Time Measurements Referenced to 1.5 V)

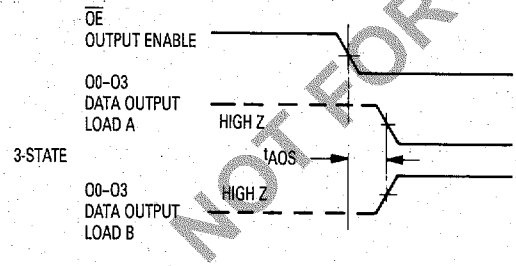
PROPAGATION DELAY FROM CHIP SELECT



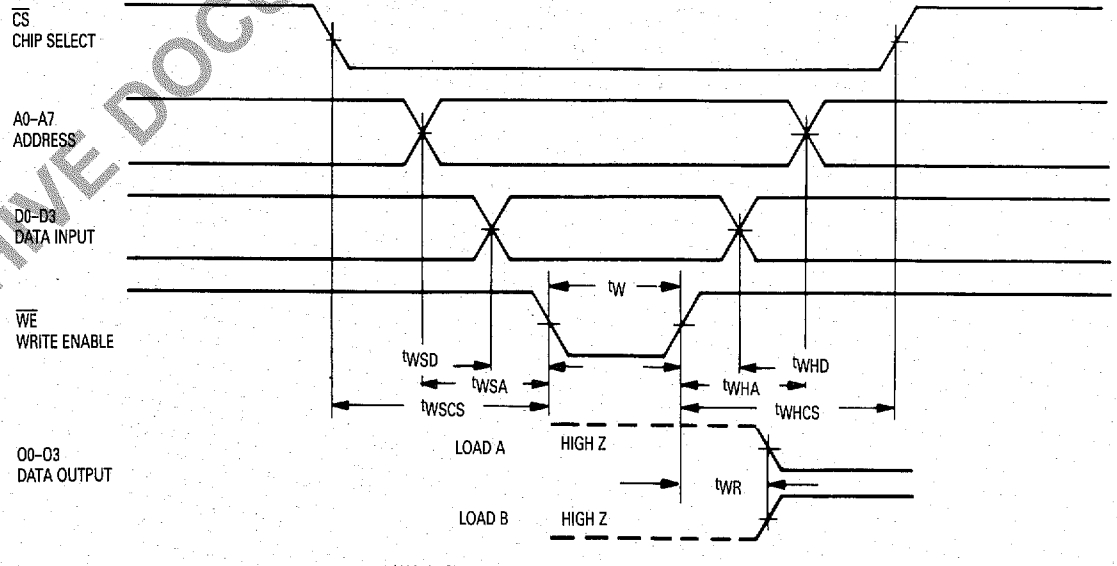
PROPAGATION DELAY FROM ADDRESS INPUTS



PROPAGATION DELAY FROM OUTPUT ENABLE

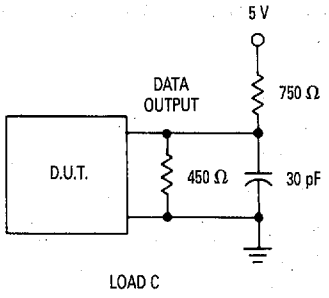


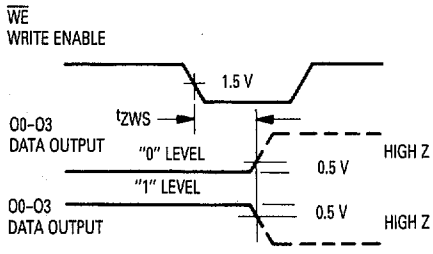
WRITE CYCLE TIMING



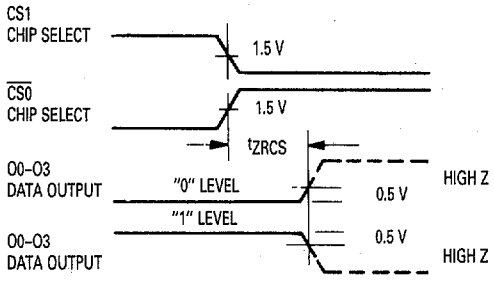
(ALL ABOVE MEASUREMENTS REFERENCE TO 1.5 V)

WRITE ENABLE TO HIGH Z DELAY

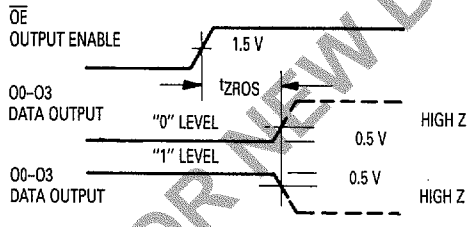




PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z



PROPAGATION DELAY FROM OUTPUT ENABLE TO HIGH Z

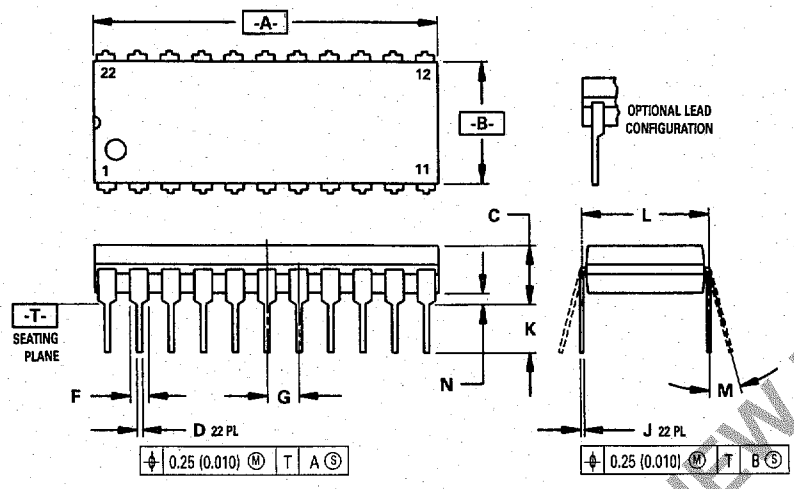


(ALL t_{ZXX} PARAMETERS ARE MEASURED AT A DELTA OF 0.5 V FROM THE LOGIC LEVEL AND USING LOAD C.)

Package	θ_{JA} (Junction to Ambient)		θ_{JC} (Junction to Case)
	Blown*	Still	
W Suffix	50°C/W	75°C/W	15°C/W

*500 linear ft. per minute blown air.

OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F FOR FULL LEADS. HALF LEADS OPTIONAL AT LEAD POSITIONS 1, 11, 12, AND 22.
5. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	26.93	27.81	1.060	1.095
B	9.15	9.90	0.360	0.390
C	3.81	5.46	0.150	0.215
D	0.39	0.53	0.015	0.021
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.39	0.008	0.015
K	3.18	4.31	0.125	0.170
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

W SUFFIX
CASE 736-05
CERAMIC PACKAGE

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