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 54/7489
 54LS/74LS89 011749

64-BIT RANDOM ACCESS MEMORY (With Open-Collector Outputs)

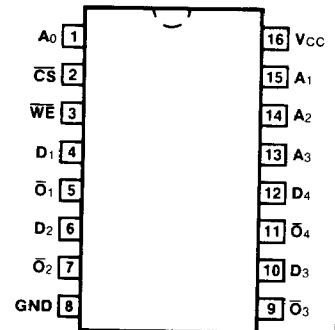
DESCRIPTION — The '89 a high speed, low power 64-bit Random Access Memory organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading, and addresses are fully decoded on-chip. Outputs are open-collector type and are in the off (HIGH) state when both the Chip Select (\overline{CS}) and Write Enable (\overline{WE}) are HIGH. For all other combinations of \overline{CS} and \overline{WE} the outputs are active, presenting the complement of either the stored data (READ mode) or the information present on the D inputs.

- OPEN-COLLECTOR OUTPUTS FOR WIRED-AND APPLICATIONS
- BUFFERED INPUTS MINIMIZE LOADING
- ADDRESS DECODING ON-CHIP
- DIODE CLAMPED INPUTS MINIMIZE RINGING

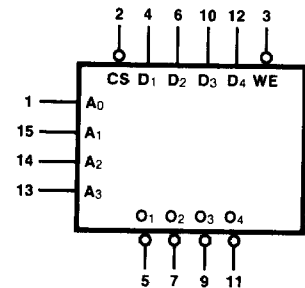
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$, $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	7489PC, 74LS89PC		9B
Ceramic DIP (D)	A	7489DC, 74LS89DC	5489DM, 54LS89DM	7B
Flatpak (F)	A	7489FC, 74LS89FC	5489FM, 54LS89FM	4L

CONNECTION DIAGRAM PINOUT A



LOGIC SYMBOL



$V_{CC} = \text{Pin } 16$
 $GND = \text{Pin } 8$

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$A_0 - A_3$	Address Inputs	1.0/1.0	0.5/0.013
\overline{CS}	Chip Select Input (Active LOW)	1.0/1.0	0.5/0.013
\overline{WE}	Write Enable Input (Active LOW)	1.0/1.0	0.5/0.013
$D_1 - D_4$	Data Inputs	1.0/1.0	0.5/0.013
$\overline{O}_1 - \overline{O}_4$	Inverted Data Outputs	OC*/7.5	OC*/10 (5.0)

*OC — Open Collector

IMAGE UNAVAILABLE

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I _{OH}	Output HIGH Current	20		20		μA	V _{CC} = Min, V _{OH} = 5.5 V
V _{OL}	Output LOW Voltage	0.4				V	V _{CC} = Min
		0.45				V	
		XM, XC			0.4		V
XC			0.5		V		
I _{CC}	Power Supply Current	105		40		mA	V _{CC} = Min, \overline{CS} = Gnd
C _o	Off-State Output Capacitance	4.0*		4.0*		pF	V _O = 2.4 V, f = 1 MHz

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		C _L = 30 pF		C _L = 15 pF			
		R _L = 300 Ω		R _L = 2 kΩ			
		Min	Max	Min	Max		
t _{PLH}	Propagation Delay	50		10*		ns	Figs. 3-2, 3-5 '89 has 600 Ω to Gnd
t _{PHL}	\overline{CS} to \overline{O}_n	50		10*			
t _{PLH}	Propagation Delay	60		37*		ns	Figs. 3-2, 3-20 '89 has 600 Ω to Gnd
t _{PHL}	A _n to \overline{O}_n	60		37*			
t _{rec}	Recovery Time	70		30*		ns	Figs. 3-2, 3-4, 3-5 '89 has 600 Ω to Gnd
	\overline{WE} to \overline{O}_n						

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t _s (H)	Setup Time HIGH or LOW	40		25*		ns	Fig. 3-13
t _s (L)	D _n to \overline{WE}	40		25*			
t _s (H)	Setup Time HIGH or LOW	0		10*		ns	Fig. 3-21
t _s (L)	A _n to \overline{WE}	0		10*			
t _h (H)	Hold Time HIGH or LOW	5.0		0*		ns	Figs. 3-13, 3-21
t _h (L)	D _n or A _n to \overline{WE}	5.0		0*			
t _w (L)	\overline{WE} Pulse Width LOW	40		25*		ns	Fig. 3-21

*Typical Value

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